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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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09/973,133

10/09/2001

Shunpei Yamazaki

SEL 281

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7590

07/12/2004

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EXAMINER

KEBEDE, BROOK

ART UNIT

PAPER NUMBER

2823

DATE MAILED: 07/12/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Applicant(s)

09/973,133

Applicant(s)

YAMAZAKI ET AL.

Examiner

Brook Kebede

Art Unit

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 26 April 2004.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 3,9-11,17-19,33-35,37-39,41-43 and 59 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 3,9-11,17-19,33-35,37-39,41-43 and 59 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date: _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claims 9-11, 17-19, 33-35, 37-39, 41-43, and 59-63 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Claims 9, 17, 33, 37, and 41 recite the limitation “a first voltage and a second voltage are **alternatively** applied between the anode and the cathode.” However, there is no support for “**alternative application**” of first and second voltages in the specification or the drawings as originally filed.

Claims 9, 17, 33, 37, and 41 recite the limitation “a difference between the first voltage and the second voltage gradually increases with time.” However, there is no support for the newly added limitation in the specification or the drawings as originally filed.

Therefore, the claims contain the subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Claims 10, 11, 18, 19, 34, 35, 38, 39, 42, 43, and 59-63 are also rejected as being dependent of the rejected independent base claim.

Double Patenting

3. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

4. Claims 9-12, 17-20, 33-44, and 59-63 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims of copending Application No. 10/158,658. Although the conflicting claims are not identical, they are not patentably distinct from each other because of the following reasons:

Re claims 9-12, 17-20, 33-44, and 59-63 the subject matter of the claimed limitation fully claimed in the subject matter of claimed limitations of claims 1-87 of co-pending application 09/158,658.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 9, 11, 17, 19, 33, 35, 37, 39, 41, 43, and 59-63 are rejected under 35

U.S.C. 102(b) as being anticipated by Tang et al. (EP/0704912).

Re claim 9, Tang et al. disclose method of repairing a light emitting device comprising a step of: applying a first voltage and a second voltage in order between an anode and a cathode of the light emitting device, wherein the anode and the cathode are located in a light emitting element with a light emitting layer interposed therebetween, and wherein the first voltage and the second voltage are reverse bias voltages of different levels; and a difference between the first voltage and the second voltage gradually increases with time (see Fig. 4) (see Tang et al. Pages 2-11;).

Re claim 11, as applied to claim 9 above, Tang et al. disclose all the claimed limitations including the limitation wherein the light emitting element is an electro-luminescence element (see Tang et al. Pages 2-11).

Re claim 17, Tang et al. disclose a method of repairing a light-emitting device comprising a step of: applying a first voltage and a second voltage in order between an anode and a cathode of the light-emitting device thereby making a portion where a reverse-bias current flows between the anode and the cathode insulating or highly resistive, and wherein the anode and the cathode are located in a light emitting- element with a light emitting layer interposed therebetween, and wherein the first voltage and the second voltage are reverse bias voltages of different levels (see Fig. 4) (see Tang et al. Pages 2-11).

Re claim 19, as applied to claim 17 above, Tang et al. disclose all the claimed limitations including the limitation wherein the light emitting element is an electro-luminescence element (see Tang et al. Pages 2-11).

Re claim 33, Tang et al. disclose a method of repairing a light-emitting device comprising a step of: applying a first voltage and a second voltage in order between an anode and a cathode of the light emitting device wherein the anode and the cathode are located in a light-emitting element with a light-emitting layer interposed therebetween, and wherein the first voltage is a ground voltage while the second voltage is a reverse bias voltage (see Tang et al. Pages 2-11).

Re claim 32, as applied to claim 33 above, Tang et al. disclose all the claimed limitations including the limitation wherein the light-emitting element is an electro-luminescence element (see Tang et al. Pages 2-11).

Re claim 37, Tang et al. disclose a method of repairing a light emitting device comprising a step of, gradually changing a voltage applied between an anode and an cathode of the light emitting device from a first voltage to a second voltage, wherein the anode and the cathode are located in a light-emitting element with a light emitting layer interposed therebetween, and wherein one of the first voltage and the second voltage is a ground voltage while the other is a reverse bias voltage (see Tang et al. Pages 2-11).

Re claim 39, as applied to claim 37 above, Tang et al. disclose all the claimed limitations including the limitation wherein the light-emitting element is an electro-luminescence element (see Tang et al. Pages 2-11).

Re claim 41, Tang et al. disclose a method of repairing a light emitting device comprising a step of: applying a first voltage and a second voltage in order between an anode and a cathode of the light emitting device, thereby making a portion where a reverse-bias current flows between the anode and the cathode, and wherein the anode, and the cathode are located in a light emitting element with a light emitting layer interposed therebetween, and wherein the first

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voltage is a ground voltage while the second voltage is a reverse bias voltage (see Tang et al. Pages 2-11).

Re claim 43, as applied to claim 41 above, Tang et al. disclose all the claimed limitations including the limitation wherein the light-emitting element is an electro-luminescence element (see Tang et al. Pages 2-11).

Re claims 59-63, as applied to claims 9, 17, 33, 37, and 49 respectively above, Tang et al. disclose all the claimed limitation including the limitation wherein the light emitting layer comprises a defection portion (i.e., pin holes) (see Tang et al. Pages 2-11).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

8. Claims 10, 18, 34, and 42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tang et al. (EP/0704912).

Re claim 10, as applied to claim 9 above, Tang et al. disclose all the claimed limitations except wherein the first voltage and the second voltage are within $\pm 1.5\%$ of an avalanche voltage of the light emitting element.

However, selection of the first and second voltage within $\pm 1.5\%$ of an avalanche voltage of the light emitting element would have been achieved by ordinary skill in the art because if excess voltage selected it may cause stress and breakdown of the TFT (thin film transistor) which is an integral part of EL. Therefore, it is desirable to optimize the voltage within desired range so that such breakdown will not be occurred.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to select the first and second voltage within $\pm 1.5\%$ of an avalanche voltage of the light emitting element because if excess voltage selected it may cause stress and breakdown of the TFT (thin film transistor) which is an integral part of EL and it is desired to optimize the voltage within desired range so that such breakdown will not be occurred, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller*, 105 USPQ 233. Furthermore, the specification contains no disclosure of either the critical nature of the claimed voltage or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. See *In re Woodruff*, 919, f.2d 1575, 1578, 16 USPQ2d, 1936 (Fed. Cir. 1990).

Re claim 18, as applied to claim 17 above, Tang et al. disclose all the claimed limitations except wherein the first voltage and the second voltage are within $\pm 1.5\%$ of an avalanche voltage of the light emitting element.

However, selection of the first and second voltage within $\pm 1.5\%$ of an avalanche voltage of the light emitting element would have been achieved by ordinary skill in the art because if excess voltage selected it may cause stress and breakdown of the TFT (thin film transistor) which is an integral part of EL. Therefore, it is desirable to optimize the voltage within desired range so that such breakdown will not be occurred.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to select the first and second voltage within $\pm 1.5\%$ of an avalanche voltage of the light emitting element because if excess voltage selected it may cause stress and breakdown of the TFT (thin film transistor) which is an integral part of EL and it is desired to optimize the voltage within desired range so that such breakdown will not be occurred, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller*, 105 USPQ 233. Furthermore, the specification contains no disclosure of either the critical nature of the claimed voltage or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. See *In re Woodruff*, 919, f.2d 1575, 1578, 16 USPQ2d, 1936 (Fed. Cir. 1990).

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Re claim 34, as applied to claim 33 above, Tang et al. disclose all the claimed limitations except wherein the first voltage and the second voltage are within $\pm 1.5\%$ of an avalanche voltage of the light emitting element.

However, selection of the first and second voltage within $\pm 1.5\%$ of an avalanche voltage of the light emitting element would have been achieved by ordinary skill in the art because if excess voltage selected it may cause stress and breakdown of the TFT (thin film transistor) which is an integral part of EL. Therefore, it is desirable to optimize the voltage within desired range so that such breakdown will not be occurred.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to select the first and second voltage within $\pm 1.5\%$ of an avalanche voltage of the light emitting element because if excess voltage selected it may cause stress and breakdown of the TFT (thin film transistor) which is an integral part of EL and it is desired to optimize the voltage within desired range so that such breakdown will not be occurred, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller*, 105 USPQ 233. Furthermore, the specification contains no disclosure of either the critical nature of the claimed voltage or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. See *In re Woodruff*, 919, f.2d 1575, 1578, 16 USPQ2d, 1936 (Fed. Cir. 1990).

Re claim 38, as applied to claim 37 above, Tang et al. disclose all the claimed limitations except wherein the first voltage and the second voltage are within $\pm 1.5\%$ of an avalanche voltage of the light emitting element.

However, selection of the first and second voltage within $\pm 1.5\%$ of an avalanche voltage of the light emitting element would have been achieved by ordinary skill in the art because if excess voltage selected it may cause stress and breakdown of the TFT (thin film transistor) which is an integral part of EL. Therefore it is desirable to optimize the voltage within desired range so that such breakdown will not be occurred.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to select the first and second voltage within $\pm 1.5\%$ of an avalanche voltage of the light emitting element because if excess voltage selected it may cause stress and breakdown of the TFT (thin film transistor) which is an integral part of EL and it is desired to optimize the voltage within desired range so that such breakdown will not be occurred, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller*, 105 USPQ 233. Furthermore, the specification contains no disclosure of either the critical nature of the claimed voltage or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. See *In re Woodruff*, 919, f.2d 1575, 1578, 16 USPQ2d, 1936 (Fed. Cir. 1990).

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Re claim 42, as applied to claim 41 above, Tang et al. disclose all the claimed limitations except wherein the first voltage and the second voltage are within $\pm 1.5\%$ of an avalanche voltage of the light emitting element.

However, selection of the first and second voltage within $\pm 1.5\%$ of an avalanche voltage of the light emitting element would have been achieved by ordinary skill in the art because if excess voltage selected it may cause stress and breakdown of the TFT (thin film transistor) which is an integral part of EL. Therefore it is desirable to optimize the voltage within desired range so that such breakdown will not be occurred.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to select the first and second voltage within $\pm 1.5\%$ of an avalanche voltage of the light emitting element because if excess voltage selected it may cause stress and breakdown of the TFT (thin film transistor) which is an integral part of EL and it is desired to optimize the voltage within desired range so that such breakdown will not be occurred, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller*, 105 USPQ 233. Furthermore, the specification contains no disclosure of either the critical nature of the claimed voltage or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. See *In re Woodruff*, 919, f.2d 1575, 1578, 16 USPQ2d, 1936 (Fed. Cir. 1990).

Response to Arguments

9. Applicants' arguments filed on April 26, 2004 have been fully considered but they are not persuasive.

With respect to claims rejection under 35 U.S.C. 102, applicants argued that "the independent claims 9, 17, 33, 37 and 41 has been amended to include the features that (1) a first voltage and a second voltage are alternatively applied between the anode and the cathode, and (2) a difference between the first voltage and the second voltage gradually increases with time."

In response to applicants' argument, the examiner respectfully submits that the argument is moot because of the new grounds of rejection as set forth in Paragraph 2 that was necessitated by the limitation that applicants believe that Tang et al. fail to teach.

However, the examiner respectfully would like to point out (since applicants are relied on Fig. 1B for support of added claims) Fig. 1B of the instant application does not show either "a first voltage and a second voltage are alternatively applied between the anode and the cathode" or "a difference between the first voltage and the second voltage gradually increases with time." On the contrary, Fig. 1B of the instant application as depicted below shows the current flow between the ground and avalanche voltage.

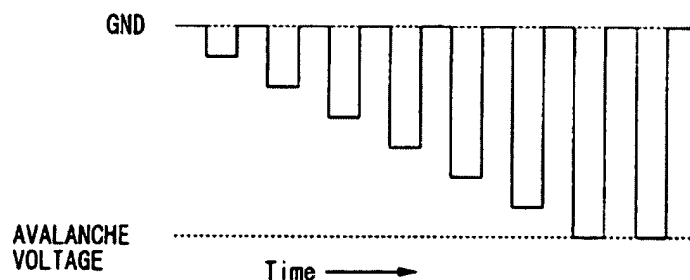


FIG. 1B

Furthermore, the newly added limitations are included in the rejected claim as set forth in Paragraph 6 and anticipated by Tang et al. as disclosed in Fig. 4.

Therefore, rejection under 35 U.S.C. 102 is deemed proper. In addition, the *prima facie* case of obviousness has been met and the rejection under 35 U.S.C. § 103 is also deemed proper as set forth in Paragraph 8 above.

Conclusion

10. Applicants' amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

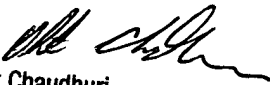
Correspondence

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brook Kebede whose telephone number is (571) 272-1862. The examiner can normally be reached on 8-5 Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on (571) 272-1855. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

BK
July 4, 2004


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